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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,623	07/02/2004	Andrew MG Westcott	540-508	2994

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EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	PAPER NUMBER
2836	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,623	WESTCOTT, ANDREW MG	
	Examiner	Art Unit	
	CARLOS AMAYA	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,9-11,13-34 and 38-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,9-11,13-34 and 38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amendments filed on 11/24/2008.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,6, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Wilcox (US 5,847,554).

With respect to claims 1, 6 Dyer discloses a pulse width modulation switching circuit, responsive to a voltage demand signal, for controlling current supplied to an inductor from a direct (DC) supply voltage, said switching circuit comprising a bridge circuit (see figure 1), said bridge circuit comprising: an input operable to receive a direct current, DC (bank battery 7), supply of nominal voltage +VS (battery 7 supplies the voltage for the input), an output, said output having opposed ends (outputs are generated at opposed end points A and B); first and second bride arms, said arms having corresponding first and second switches (Switches 21 and 19 of first and second arms respectively connected to opposed ends to the output) operable in response to first and second switching signals to be switched between on and off states (controller 29 in conjunction with driver circuits 31 and 32 supplies the signal for the switches to

turn on and off, column 4 lines 24-37), wherein switching between various combinations of on and off states produces an electrical signal at the opposed ends of said output with voltage pulses at levels of nominally +VS, 0V and -VS (The turning on and off of the transistor produces a desired output as can be better seen in figure 3); controller 29 generates a signal to control the operation of the switches according to a demand signal.

Dyer, however, does not disclose expressly a voltage sensor for producing a signal indicative of said DC supply voltage; and a switching signal generator, responsive to said DC supply voltage signal and said voltage demand signal, for generating said first and second switching signals.

Wilcox discloses voltage sensing circuit 320 for sensing the voltage drop of the transistor, which is an indication of the current supplied by the regulator and the DC input Vin, see abstract. Figure 3 shows oscillator 104, latch 106, drivers 108 and 112, and sensing circuit 320 to control the switching signals provided to switches 342 and 344.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Dyer with the voltage sensor disclosed by Wilcox, col. 5 lines 1-42.

The suggestion or motivation for doing so would have been to avoid dissipative losses in current sensing elements and costly manufacturing process, col. 5 lines 37-42.

With respect to claims 9-11 Dyer in view of Wilcox disclose the switching circuit according to claim 1. Dyer discloses that the bridge circuit is a half-bridge with third and

fourth arms having diodes (Column 3 lines 40-41, line 45). The first and second switches are transistors (Transistor switching device 19 and 21). Comprising an electromagnet connected across the output of the bridge circuit (Figure 1 Inductor 5).

4. Claims 1,6, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Kern (US 6,081,104).

With respect to claims 1, 6 Dyer discloses a pulse width modulation switching circuit (pulse timing circuits 51, 53), responsive to a voltage demand signal, for controlling current supplied to an inductor from a direct (DC) supply voltage, said switching circuit comprising a bridge circuit (see figure 1), said bridge circuit comprising: an input operable to receive a direct current, DC (bank battery 7), supply of nominal voltage +VS (battery 7 supplies the voltage for the input), an output, said output having opposed ends (outputs are generated at opposed end points A and B); first and second bride arms, said arms having corresponding first and second switches (Switches 21 and 19 of first and second arms respectively connected to opposed ends to the output) operable in response to first and second switching signals to be switched between on and off states (controller 29 in conjunction with driver circuits 31 and 32 supplies the signal for the switches to turn on and off, column 4 lines 24-37), wherein switching between various combinations of on and off states produces an electrical signal at the opposed ends of said output with voltage pulses at levels of nominally +VS, 0V and -VS (The turning on and off of the transistor produces a desired output as can be better

seen in figure 3); controller 29 generates a signal to control the operation of the switches according to a demand signal.

Dyer, however, does not disclose expressly a voltage sensor for producing a signal indicative of said DC supply voltage; and a switching signal generator, responsive to said DC supply voltage signal and said voltage demand signal, for generating said first and second switching signals.

Kern discloses a DC input voltage sensor 58 for sensing the input voltage and producing a signal to a controller 82; controller 82 in turn produces a signal to control the switches of the power converter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the invention disclosed by Dyer to include the voltage sensor 58 to supply a signal indicative of the DC supply, for the purpose of obtaining a desired output based on the available supply (col. 7 lines 42-47).

With respect to claims 9-11 Dyer in view of Kern disclose the switching circuit according to claim 1. Dyer discloses that the bridge circuit is a half-bridge with third and fourth arms having diodes (Column 3 lines 40-41, line 45). The first and second switches are transistors (Transistor switching device 19 and 21). Comprising an electromagnet connected across the output of the bridge circuit (Figure 1 Inductor 5).

Response to Arguments

5. Applicant's arguments filed 11/24/2008 have been fully considered but they are not persuasive.

With respect to the argument that Wilcox voltage sensing circuit 320 does not meet the claim, please note that the sensor claimed only needs to produce a signal **indicative** of the supply voltage. As clearly shown in the connections of figure 3, voltage sensor 320 produces a signal indicative of Vin. Furthermore, as with the argument that the voltage drop across the transistors it is not sensed simultaneously, please see col. 4 lines57-67; col. 5 lines 61-67. Wilcox discloses voltage sensing circuit 320 for sensing the voltage drop of the transistor, which is an indication of the current supplied by the regulator and the DC input Vin, see abstract. Figure 3 shows oscillator 104, latch 106, drivers 108 and 112, and sensing circuit 320 to control the switching signals provided to switches 342 and 344.

With respect to the argument that "In Kern, the only reason for having a voltage sensor is to determine whether or not power is available". Please note that the sensor claimed only needs to produce a signal **indicative** of the supply voltage. Furthermore, Kern discloses that controller 82 provides PWM logic signals to the switches (see figures 1,5,11).

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 13-20, 23-34 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 7,187,567. Although the conflicting claims are not identical, they are not patentably distinct from each other because.

With respect to claims 13, 40, claims 1, 7, 12 of Patent (US 7,187,567) disclose the limitations of claims 13 and 40. NOTE: claim 7 teaches PWM, and claim 12 teaches generating the switching signals with reference to a voltage signal indicative of the DC supply voltage.

With respect to claim 14, claim 12 of Patent (US 7,187,567) disclose the limitations of claim 14.

With respect to claim 15, claim 13 of Patent (US 7,187,567) disclose the limitations of claim 15.

With respect to claim 16, claim 14 of (US 7,187,567) discloses the switching circuit as claimed in claimed 16.

With respect to claim 17, claim 15 of (US 7,187,567) discloses the switching. circuit as claimed in claimed 17.

With respect to claim 18, claim 16 of (US 7,187,567) discloses the switching circuit as claimed in claimed 18.

With respect to claim 19, claim 17 of (US 7,187,567) discloses the switching circuit as claimed in claimed 19.

With respect to claim 20, claim 25 of (US 7,187,567) discloses the switching circuit as claimed in claimed 20.

With respect to claim 23, claim 2 of (US 7,187,567) discloses the switching circuit as claimed in claimed 23.

With respect to claim 24, claim 3 of (US 7,187,567) discloses the switching circuit as claimed in claimed 24.

With respect to claim 25, claim 4 of (US 7,187,567) discloses the switching circuit as claimed in claimed 25.

With respect to claim 26, claim 5 of (US 7,187,567) discloses the switching circuit as claimed in claimed 26.

With respect to claim 27, combination of claims 1-6 of (US 7,187,567) discloses the switching circuit as claimed in claimed 27.

With respect to claim 28, claim 7 of (US 7,187,567) discloses the switching circuit as claimed in claimed 28.

With respect to claim 29, claim 18 of (US 7,187,567) discloses the switching circuit as claimed in claimed 29.

With respect to claim 30, claim 20 of (US 7,187,567) discloses the switching circuit as claimed in claimed 30.

With respect to claim 31, claim 1 of (US 7,187,567) discloses the switching circuit as claimed in claimed 31.

With respect to claim 32, claim 1 of (US 7,187,567) discloses the switching circuit as claimed in claimed 31.

With respect to claim 33, claim 23 of (US 7,187~567) discloses the switching circuit as claimed in claimed 33.

With respect to claim 34, claim 24 of (US 7,187,567) discloses the switching circuit as claimed in claimed 33.

Please note: Claims 13, 27, and 40 and the claims that dependent on them would be allowable except for the double patent rejection above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARLOS AMAYA whose telephone number is (571) 272-8941. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A./
Examiner, Art Unit 2836

/Albert W Paladini/ 2/27/09
Primary Examiner, Art Unit 2836